SEMICONDUCTOR DEVICE CAPABLE OF PREVENTING A PATTERN COLLAPSE

Field of the Invention

The present invention relates to a semiconductor device; and, more particularly, to a semiconductor device capable of preventing a pattern collapse in an edge area in a semiconductor wafer.

Description of Related Art

There are some incidentally occurring problems in manufacturing processes as a semiconductor device is highly integrated, and one of which is a pattern defect generated in a cell edge area of a semiconductor memory device.

For instance, in such manufacturing process for forming multiple patterns like isolated bar-type pattern composing the semiconductor device, a pattern formation process is enforced to minimize a proximity effect generated in a cell edge area during a photo-lithography process. Herein, as the proximity effect is a kind of skin effects, meaning that a density of a current flowing through each conductive material is changed in response to a direction, amount, or a frequency of the current when a plurality of the conductive materials are closely arranged. For an effective pattern formation in cell edge area, dummy patterns are formed in the same manner of forming line patterns in the cell edge area.

Due to a current trend of high integration of the semiconductor device, bar-type patterns are formed in the cell edge area through the same condition of forming the line patterns in a cell center area in order to improve line width uniformity.

It is an object of the present invention to provide a semiconductor device capable of preventing a pattern collapse phenomenon in an area, where a pattern becomes fragile, for instance, in a cell edge area.

Summary of the Invention

In accordance with an aspect of the present invention, the inventive semiconductor device having a lower pattern density in an edge area than in a central area of a wafer includes a plurality of bar-type patterns allocated at a predetermined distance in the central area of the wafer; a plurality of dummy patterns formed in the edge area; and a plurality of a connection pattern for coupling at least two of the bar-type patterns to each other, wherein the connection patterns of the plurality of dummy patterns is allocated in a zigzag fashion.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description

of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plane view illustrating bar-type patterns formed in cell center and edge areas of a conventional semiconductor device;

Fig. 2 is a diagram showing a pattern collapse phenomenon in the cell edge area of the conventional semiconductor device;

Fig. 3 is a diagram of a scanning electron microscope SEM micrograph showing a plane view of the pattern collapse of a dummy pattern in the cell edge area o the conventional semiconductor device;

Figs. 4A and 4B are diagrams of SEM micrographs showing the pattern collapse of the bar pattern in the cell edge area;

Fig. 5 is a plane view of a semiconductor device completed with a predetermined process for forming a bar pattern in accordance with a preferred embodiment of the present invention; and

Fig. 6 is a diagram of a SEM micrograph showing a plane view of the semiconductor device described in Fig. 5.

Detailed Description of the Invention

Referring to FIGS. 1-4B, a conventional semiconductor device is generally shown. Fig. 1 is a plane view illustrating bar-type patterns formed in cell center and edge areas of a conventional semiconductor device. Fig. 2 is a

explanatory diagram for describing a pattern collapse in the cell edge area of the conventional semiconductor device, and Fig. 3 is a diagram of a scanning electron microscope SEM micrograph showing a plane view of the pattern collapse of a dummy pattern in the cell edge area in where the bar-type patterns are formed.

As shown in Fig. 1, a plurality of the bar-type patterns 10A are formed with a predetermined distance d in the cell center and edge areas. A plurality of the dummy patterns 10B are formed in the cell edge area.

The function of the dummy pattern 10B is to help form a main pattern, and it is very important and certainly necessary for preventing a collapse of the main pattern.

However, for a device of which the minimum feature size is below about 100 nm, a thickness of a photo-resist must be increased with a consideration of etch resistance for a line width. The pattern collapse is a more critical issue at the isolated bar-type pattern than at a straight pattern. Pattern collapse generally occurs in a case that a ratio of a thickness of the photo-resist to a critical dimension is under 3:1. Especially, the repeated dummy patterns 10B originally designed to be the same size of the pattern formed throughout the cell area become smaller because of the proximity effect in the cell edge area, referring to a reference numeral '11' shown in Fig. 2. As a result, the pattern collapse, referring to a reference numeral '12' shown in Fig. 3, of the photo-resist becomes more critical.

Figs. 4A and 4B are diagram of SEM micrographs showing the pattern collapse of the bar pattern in the cell edge area. As shown, it is possible to confirm that the dummy pattern 10B collapse in cell edge area in several forms due to the proximity effect.

Referring to FIGS. 5 and 8, a semiconductor device capable of preventing pattern collapse in accordance with the present invention is generally shown. The present invention is designed under the basic principle that a pattern collapse phenomenon can be effectively overcome in case that a contact surface area between a pattern and a lower layer, e.g., an insulation layer, is large. For minimizing a proximity effect that occurs in a cell edge area by limitation of photo-lithography, at least several to dozens of dummy patterns are formed in the cell edge area and these dummy patterns have a similar site to bar-patterns formed in the whole cell area. Also, there are conditions to form effectively isolated bar-patterns minimized with the proximity effect. First, isolated bar patterns formed in the cell edge area are the dummy patterns. Furthermore, dummy patterns are regularly connected to each other in order to effectively present the pattern collapse among the dummy patterns and increase the contact surface area of the bar-pattern with the lower layer.

Hereinafter, a semiconductor device according to the present invention will be described in detail referring to the accompanying drawings.

Fig. 5 is a plane view of a semiconductor device

completed with a predetermined process for forming a bar pattern in accordance with a preferred embodiment of the present invention.

As shown, in the inventive semiconductor device, there is a semiconductor memory cell 50 of which size gets smaller because the bar-pattern has less topology in a cell edge area B-B' than in a cell center area A-A'. The semiconductor memory device includes a plurality of the bar-type patterns 51 formed in the cell center area A-A' except for the cell edge area B-B', and a connection pattern 52C connecting at least two bar-type patterns 52A and 52B to each other for protecting the bar patterns 52A and 52B from being collapsed. Herein, the bar-type patterns 52A and 52B are formed in the cell edge area B-B' of the semiconductor memory cell 50. Also, the bar-type patterns 52A and 52B and the connection pattern 52c are a dummy pattern.

It is also noted that the cell edge area B-B' has a lower topology because of a lower pattern density in the cell edge area B-B' than in the cell center area A-A'.

The dummy pattern is formed through the use of the same photo-lithography using the same material for the bar-type pattern 51 in the cell center area A-A'. The cell edge area B-B' can be called a dummy area.

The bar-type pattern 51 is typically used not only in a landing plug contact LPC process for making a plug contacted to an active area of a wafer but also in a device isolation process.

The dummy patterns, more concretely, the bar-type patterns 52A and 52B in the cell edge area B-B', have the same size of the bar-type pattern 51 in the cell center area A-A'. Particularly, the allowable size of the dummy pattern ranges from about 80% to about 120% of the bar-type pattern 51 size.

It is possible to apply this approach to a core memory area and a periphery area in addition to the cell center area A-A' and the cell edge area B-B'.

As shown in Fig. 5, the bar-type patterns 52A and 52B have less adhesive force to the layer beneath than those in the cell center area A-A'. The dummy patterns produced by connecting at least the two bar-type patterns 52A and 52B to each other throughout the connection pattern 52C for increasing the contact surface area with the lower layer enhance the adhesive force. The connection pattern 52C is not a straight pattern but a zigzag pattern. Namely, a plurality of the connection pattern 52C is allocated in zigzags for connecting the two bar-type patterns in the cell edge area B-B'.

Thus, it is possible to minimize the pattern collapse occurred by the proximity effect.

Fig. 6 is a diagram of a SEM micrograph showing a plane view of the semiconductor device described in Fig. 5.

As shown, there are formed a plurality of the dummy patterns of which surface area contacted to the lower layer is increased by connecting the two bar-type patterns 52A and 52B to each other throughout the use of the connection pattern 52C

in the cell edge area B-B'.

As verified from Fig. 6, the pattern collapse is not occurred by forming the dummy pattern in the cell edge area B-B' with the specific design described in Fig. 5.

In accordance with the preferred embodiment of the present invention, the bar-type dummy patterns are formed by connecting at least two bar-type patterns through the use of the connection pattern in the cell edge area to thereby increase the contact area of the bar-type dummy patterns with the lower layer. This increased contact area provides a further effect of preventing the pattern collapse in the cell edge area.

For example, the preferred embodiment of the present invention provides an example of a cell using a device isolation layer and a landing plug contact as the bar-type pattern. However, the bar-type pattern can be also applied not only to a conductibility pattern such as a bit line, a word line, a metal wire, and so on but also to other various types of patterns.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modification may be made without departing from the spirit and scope of the invention as defined in the following claims.